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Total No. of Questions—12]

[Total No. of Printed Pages—4+1

**[4062]-203**

**S.E. (Common to IT) (Computer Engineering)**

**(First Semester) EXAMINATION, 2011**

**DIGITAL ELECTRONICS AND LOGIC DESIGN**

**(2008 PATTERN)**

**Time : Three Hours**

**Maximum Marks : 100**

**N.B. :—** (i) Answers to the two Sections should be written in separate answer-books.

(ii) In Section I Attempt : Q. No. 1 or Q. No. 2,  
Q. No. 3 or Q. No. 4, Q. No. 5 or Q. No. 6.

In Section II Attempt : Q. No. 7 or Q. No. 8,  
Q. No. 9 or Q. No. 10, Q. No. 11 or Q. No. 12.

(iii) Neat diagrams must be drawn wherever necessary.

(iv) Figures to the right indicate full marks.

(v) Assume suitable data, if necessary.

**SECTION I**

1. (a) Do the required conversions for the following numbers : [6]

(i)  $(BF8)_{16} = (\quad)_{10}$

(ii)  $(1000)_{10} = (\quad)_8$

(iii)  $(377)_8 = (\quad)_{16}$

(b) What are different ways of representing signed binary numbers ? Explain with examples. [6]

(c) Solve the following equation using K map minimization technique.

Draw the diagram for the output : [6]

$$Z = f(A, B, C, D) = \pi M(0, 1, 6, 7, 8, 9).$$

P.T.O.

Or

2. (a) Perform the following operations : [8]

(i)  $(FFFF)_{16} - (10000)_{10} = (\text{ })_{10}$

(ii)  $(765)_8 + (365)_8 = (\text{ })_{16}$

(iii)  $(658)_{16} + (975)_{16} = (\text{ })_{16}$

(iv)  $(1011.101)_2 = (\text{ })_{10}$

(b) Solve the following equation using corresponding minimization technique. Draw the diagram for the output : [6]

$$Z = f(A, B, C, D) = \Sigma m(2, 4, 6, 11, 12, 14) + d(3, 10).$$

(c) What are the advantages of Quine McClusky minimization technique over K map ? [4]

3. (a) Define the following terms related to logic families. Mention typical values for standard TTL family : [8]

(i) Propagation delay

(ii) Fan-out

(iii)  $V_{IL}$ ,  $V_{IH}$

(iv) Noise margin.

(b) Draw the structure of two input CMOS NAND gate. Explain its working. [4]

(c) List differences between CMOS and TTL. [4]



Or

4. (a) Explain the working of two input TTL NAND gate with open collector output. Consider various input, output states for explanation. [8]
- (b) Which specifications of logic families are significant in CMOS-TTL interfacing ? Explain the same when CMOS drives TTL. [8]
5. (a) How is BCD addition different from binary addition ? What is the use of 7483 chip ? Draw and explain nine's complementer used in BCD subtractor using 7483. [8]
- (b) Design 16 : 1 multiplexer using only one 8 : 1 multiplexer and required discrete logic gate for the following function : [8]

$$F(A, B, C, D) = \sum m(0, 4, 6, 9, 12, 13).$$

Or

6. (a) What do you mean by parity ? How does IC 74180 work ? Design 9 bit even parity generator using the same. [8]
- (b) Implement two bit comparator using 1 : 16 demultiplexer (active low output). Draw the truth table of two bit comparator and explain the design in steps. [8]

## SECTION II

7. (a) Design binary sequence generator to generate binary sequence '11010' using MS JK flip-flops. How to avoid lockout condition in designed sequence generator ? [10]
- (b) Assume 16 MHz clock source in a system. How will you divide this frequency by a factor 4 ? Explain your logic with suitable circuit diagram. [6]

Or

8. (a) Draw basic internal architecture of IC 7490. Design a divide-by-20 counter using same. [8]
- (b) Draw and explain 4 bit bidirectional shift register. [8]
9. (a) Draw an ASM chart, state table and state diagram for synchronous circuit having the following description : [10]
- "The circuit has a control input X, clock and outputs A and B. If  $X = 1$ , on every clock rising edge the code on BA changes from 00-01-10-11-00 and repeats. If  $X = 0$ , circuit holds the present state."
- (b) What is difference between signal and variable in VHDL ? Explain with example. [6]



*Or*

10. (a) Write VHDL description of full subtractor using dataflow and structural modeling. [10]  
(b) State and explain basic components of ASM chart. [6]
11. (a) Explain steps for designing circuits using CPLD. [6]  
(b) Write a short note on FPGA. [6]  
(c) Explain operations performed in various phases of instruction execution in microprocessor. [6]

*Or*

12. (a) Design 3 : 8 decoder with PLD. [6]  
(b) Draw and explain the block diagram of simple microprocessor based system. [8]  
(c) Differentiate between FPGA and CPLD. [4]