Total No of Questions: [12] *SEAT NO. :*

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S.E. 2008 (INFORMATION TECHNOLOGY)
DIGITAL ELECTRONICS & LOGIC DESIGN (210243)
(Semester - I)

Time: 3 Hours *Max. Marks : 100*

Instructions to the candidates:

1) ***Answer Q.1 or Q.2 , Q.3 or Q.4 ,Q.5 or Q.6 , Q.7 or Q.8 , Q.9 or 10 and Q.11 or Q.12***
2) ***Neat diagrams must be drawn wherever necessary.***
3) ***Figures to the right side indicate full marks.***
4) ***Assume Suitable data if necessary***

SECTION I

Q1) a) Represent $(-18)_{10}$ & $(-3)_{10}$ in 2's complement representation and Perform the following operations using 2's complement method. [10]

i. $(18)_{10} - (3)_{10}$
ii. $-(18)_{10} - (-3)_{10}$
iii. $-(18)_{10} - (3)_{10}$
iv. $(18)_{10} + (3)_{10}$

b) Code decimal number 23.45 in straight binary, Gray, BCD & Excess 3 code. [8]

OR

Q2) a) Express the following numbers in Binary, BCD, Excess 3, Octal and Hexadecimal. Show step by step calculations. [10]

i. $(32)_{10}$ ii. $(47)_{10}$

b) Implement following Boolean function with ONLY NAND gates & ONLY NOR gates. Y = AB + AC + A#BC [8]

Q3) a) Compare TTL and CMOS Logic Family by considering following Parameters. [8]

i. Noise Immunity
ii. Propagation delay
iii. Power Dissipation
iv. Fan Out

b) Draw and explain 2 inputs TTL NAND gate with Totem Pole Output. [8]

OR

Q4) a) State conditions to be satisfied for interfacing, by driving & load gate. Draw and explain the interfacing of CMOS driving TTL [8]

b) Define the following IC characteristics & write typical value for CMOS logic family [8]

i. Supply voltage and Temperature range
ii. Propagation delay
iii. Power dissipation
iv. Figure of merit

Q5) a) Design Full adder and Full Subtractor using suitable Demultiplexer. [8]

b) Minimize the following function using K-map and implement using basic logic gates $f(A,B,C,D) = \sum m(1,2,5,8,9,10,12,13) + d(3,6,7)$ [8]

OR

Q6) a) Design using 4:1 Multiplexer and Logic gates. $F = \sum m (1,2,4,9,11,14)$ [8]

b) Comment on propagation delay of parallel adder & carry look ahead adder. Write propagation delay of 4 bit parallel adder & carry look ahead adder in terms of gate delay. [8]

SECTION II

Q7) a) Explain the difference between asynchronous and synchronous counter & Convert S - R flip- flop into J – K flip- flop. Show the design. [10]

b) Draw and explain 4 bit Johnson counter. If initial state of 4 bit Johnson counter is "1000", with waveform explain all possible states from initial state. [8]

OR

Q8) a) Design a Sequence generator to generate sequence 4→1→5→2→3→4. Using Master Slave JK Flip Flop IC 7476. [10]

b) What is race around condition? Explain with the help of timing diagram. How is it removed in basic flip-flop circuit? [8]

Q9) a) Design Excess 3 to BCD code convertor using PLA. [8]

b) Draw & explain the general block diagram of PAL. [8]

OR

Q10) a) Implement the following function using programming Logic Array? [8]

F1 = m(0,3,4,7) F2 = m(1,2,5,7)

b) Differentiate between PAL & PLA and CPLD & FPGA. [8]

Q11) a) List different VHDL Modeling styles & comment on difference in them with example. [8]

b) What is bus? Explain the significance of data, address & control bus of microprocessor. [8]

OR

Q12) a) Comment on difference between 'signal' & 'variable' in VHDL. [8]

b) Draw & explain the general block diagram of microprocessor. [8]