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S.E. (Comp. Engg.) (I Sem.) (Common to IT)

EXAMINATION, 2009

DIGITAL ELECTRONICS AND LOGIC DESIGN

(2008 COURSE)

Time : Three Hours **Maximum Marks : 100**

N.B. :— (*i*) Answer questions **1** or **2**, **3** *or* **4**, **5** *or* **6** from Section I and questions **7** or **8**, **9** *or* **10**, **11** *or* **12** from Section II.

(*ii*) Answers to the two Sections should be written in separate answer-books.

(*iii*) Neat diagrams must be drawn wherever necessary.

(*iv*) Figures to the right indicate full marks.

(*v*) Assume suitable data, if necessary.

SECTION I

1. (*a*) What will be the Excess-3 code of any given 4-bit grey code number ? Show the truth table. [6]

(*b*) Express the following numbers in binary. Show your step by step equations and calculations : [6]

(*i*) $(1010.11)_{Decimal}$

(*ii*) $(428.10)_{Decimal}$.

(*c*) Perform the following Hexadecimal subtraction and show your answer in Hexadecimal only : [6]

(*i*) $(387)_{Hex} - (2AC)_{Hex}$

(*ii*) $(587)_{Hex} - (4EB)_{Hex}$.

P.T.O.

Or

2. (*a*) What is the max. equivalent decimal number represented by its max. equivalent 4-digit Hex number ? Also convert the following Hex numbers to get its equivalent octal and decimal : [8]

(*i*) $(ABC)_{Hex}$

(*ii*) $(DEF)_{Hex}$.

(*b*) What is De Morgan's theorem ? Solve the following using minimization technique : [10]

(*i*) $z = f(A, B, C, D) = \Sigma(0, 2, 4, 7, 11, 13, 15)$

(*ii*) $z = f(A, B, C, D) = \pi(1, 2, 3, 6, 8, 11, 14, 15)$.

3. (*a*) With the help of Quine-McClusky technique determine the PI for the following equation : [10]

$z = f(A, B, C, D) = \Sigma(0, 1, 3, 4, 6, 8, 10, 12, 14)$.

(*b*) Explain standard TTL characteristics in brief. [6]

Or

4. (*a*) Draw 2-i/p standard TTL NAND gate circuit and explain operation of transistor (ON/OFF) with suitable conditions and truth table. [10]

(*b*) Compare TTL and CMOS logic family. Also draw CMOS-NOR gate. [6]

5. (*a*) Draw and explain 4-bit BCD subtractor using IC 7483. Explain subtraction for $(9 - 5)_{BCD}$ and $(4 - 7)_{BCD}$. [10]

(*b*) Explain the working of magnitude comparator using IC 7485. Choose suitable inputs. [6]

Or

6. (*a*) Design 12 : 1 mux using 4 : 1 multiplexers (with enable inputs). Explain the truth table of your circuit in short. [8]

(*b*) Explain DEmux (1 : 8) as a full adder and full subtractor. Show your design. [8]

SECTION II

7. (*a*) Explain the difference between combinational and sequential circuit. Also convert J-K flip-flop into D-FF and T-FF. Show the truth table. [8]

(*b*) Draw 3-bit Asynchronous counter. Explain timing diagram for the same. [8]

Or

8. (*a*) What is MOD counter ? Explain MOD-27 counter using IC 7490. Draw design for the same. [8]

(*b*) Explain Johnson counter with design for initial state '0110'. From initial state explain and draw all possible states. [8]

9. (*a*) What is ASM chart ? Design ASM chart for 3-bit up-down counter. [8]

(*b*) What is VHDL ? Explain entity-architecture declaration for 2-bit X-NOR gate. [8]

Or

10. A sequential ring counter with present state '0001'. The circuit also have an input 'X'. If X = 0, then circuit will show next output else for X = 1 it will show initial state '0001'. Draw an ASM chart and state table for this circuit to generate the output using mux controller method. [16]

11. (*a*) Explain basic architecture of FPGA. [8]

(*b*) Explain basic microprocessor architecture. [8]

Or

12. (*a*) Explain the design model of PLA. [8]

(*b*) Explain in brief the working of Address bus, Data bus and Control bus by assuming a basic operation. [8]