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Total No. of Questions—12] [Total No. of Printed Pages—4

Seat No.	

[4262]-203

S.E. (Computer and IT) (I Sem.) EXAMINATION, 2012

DIGITAL ELECTRONICS AND LOGIC DESIGN

(2008 PATTERN)

Time : Three Hours **Maximum Marks : 100**

N.B. :— (*i*) In Section I attempt : Q. No. **1** *or* Q. No. **2**, Q. No. **3** *or* Q. No. **4**, Q. No. **5** *or* Q. No. **6**.
In Section II attempt : Q. No. **7** *or* Q. No. **8**, Q. No. **9** *or* Q. No. **10**, Q. No. **11** *or* Q. No. **12**.

(*ii*) Answers to the two Sections should be written in separate answer-books.

(*iii*) Neat diagrams must be drawn wherever necessary.

(*iv*) Figures to the right indicate full marks.

(*v*) Assume suitable data, if necessary.

SECTION I

1. (*a*) Convert the following numbers to hexadecimal form. Show the steps of conversion : [8]

(*i*) $(675.625)_{10}$

(*ii*) $(451)_8$

(*iii*) $(95.5)_{10}$

(*iv*) $(11001011101)_2$.

P.T.O.

(*b*) Convert the following numbers into equivalent decimal numbers : [8]

(*i*) $(327.4051)_8$

(*ii*) $(5A.FF)_{16}$

(*iii*) $(101110111)_2$

(*iv*) $(3FFF)_{16}$.

(*c*) Represent +40 and –40 decimal numbers using 2's complement method. [2]

Or

2. (*a*) Convert the following numbers to octal form. Show the steps of conversion : [8]

(*i*) $(111110001.10011001101)_2$

(*ii*) $(3287.51)_{10}$

(*iii*) $(0.BF85)_{16}$

(*iv*) $(1234)_{16}$.

(*b*) Minimize the following four variable functions using K-map. '*d*' represents don't care conditions : [10]

(*i*) $f(A, B, C, D) = \Sigma m(1, 3, 7, 11, 15) + d(0, 2, 5)$

(*ii*) $f(A, B, C, D) = \Pi M(4, 5, 6, 7, 8, 12) \cdot d(1, 2, 3)$.

3. (*a*) Compare TTL and CMOS logic families. [8]

(*b*) Draw and explain 2-input NAND TTL logic gate with totem output driver. [8]

Or

4. (*a*) Explain the standard TTL characteristics in detail. [8]

(*b*) Draw and explain the working of a 2-input CMOS NAND gate. [8]

5. (*a*) Implement the following expression using 8 : 1 multiplexer :

$f(A, B, C, D) = \Sigma m(2, 4, 6, 7, 9, 10, 11, 12, 15)$. [8]

(*b*) Design 2-bit magnitude comparator using logic gates. Assume that A and B are 2-bit inputs. The outputs of comparator should be A > B, A = B, A < B. [8]

Or

6. (*a*) Design 4-bit BCD to excess-3 code converter. Use logic gates as per your design and requirement. [8]

(*b*) Draw and explain 4-bit BCD adder using IC7483. Also explain with example addition of numbers with carry. [8]

SECTION II

7. (*a*) Draw and explain 3-bit asychronous UP counter. Also draw the necessary timing diagram. Compare between synchronous counter and asynchronous counter. [10]

(*b*) Design the following using IC7490 : [8]

(*i*) MOD 97 counter

(*ii*) MOD 45 counter.

Or

8. (*a*) Design sequence detector using J-K flip-flop to detect the following sequence .....1101..... [10]

(*b*) Explain serial to parallel shift register with neat circuit diagram and timing diagram. [8]

9. (*a*) What is ASM chart ? Explain MUX controller method using suitable example. [8]

(*b*) What are the important features of VHDL ? Write VHDL code for 4 : 1 multiplexer in Behavioural and Data flow modeling. [8]

Or

10. (*a*) What is VHDL ? Write VHDL code for 3 : 8 decoder using CASE statement. [8]

(*b*) Design ASM chart for 2-bit up-down counter having mode control inputs. [8]

11. (*a*) Differentiate between CPLD and FPGA. [8]

(*b*) Draw and explain basic microprocessor architecture. [8]

Or

12. (*a*) Implement 4 : 1 multiplexer using PAL. [8]

(*b*) Explain basic characteristics of FPGA. [8]